AMENDMENTS TO THE CLAIMS

Please amend the claims to read as follows:

1-10 (canceled)

11. (new) A method of processing silicon, comprising:

locally forming porous silicon in a first side of a crystalline silicon substrate by electrochemical dissolution at a current density sufficiently low to avoid electropolishing; and then

increasing the current density to form a cavity and a porous silicon membrane, the cavity disposed under the porous silicon membrane.

12. (new) The method of claim 11, further comprising:

forming a masking layer for the local porous silicon formation on the first side of the crystalline silicon substrate prior to electrochemical dissolution.

13. (new) The method of claim 11, further comprising:

forming an ohmic contact on a side of the crystalline silicon substrate opposite the first side, prior to electrochemical dissolution.

14. (new) The method of claim 11, further comprising:

depositing a thin dielectric layer over the first side of the silicon substrate, having the porous silicon membrane;

depositing and patterning a polycrystalline silicon layer over the dielectric layer, at least one portion of the patterned polycrystalline silicon lying over the cavity;

doping the polycrystalline silicon with a p-type dopant to form a resistor heater and a thermocouple;

depositing and patterning aluminum or n-doped polycrystalline silicon, to form a second thermocouple;

depositing and patterning aluminum to form pairs of metal pads and respective interconnects from the thermocouples and resistor heater to the pairs of respective metal pads, respectively, the depositing and patterning of aluminum to form the metal pads and interconnects optionally simultaneously forming the second thermocouple, if aluminum, to form a sensor.

15. (new) The method of claim 14, comprising forming a series of said first and second thermocouples.

16. (new) The method of claim 15, further comprising:

forming a passivation layer on top of the sensor, the passivation layer comprising an insulating layer.

17. (new) The method of claim 16, wherein the insulating layer comprises a material selected from the group consisting of silicon oxide, silicon nitride, and polyimide.

18. (new) The method of claim 16, wherein the thermocouples comprise hot contacts and cold contacts, and further comprising forming the polycrystalline silicon resistor and hot contacts of the two series of thermocouples over the porous silicon membrane and forming the cold contacts of the two series of thermocouples over bulk crystalline silicon.

19. (new) The method of claim 18, further comprising forming the interconnects and metal pads over bulk crystalline silicon.

20. (new) The method of claim 19, further comprising:

forming a passivation layer on top of the sensor.

21. (new) The method of claim 20, wherein the passivation layer comprises a material selected from the group consisting of silicon oxide, silicon nitride, and polyimide.

22. (new) The method of claim 11, wherein the cavity is formed in the shape of a channel and further comprising:

depositing a thin silicon dioxide layer over the first side of the silicon substrate, having the porous silicon layer;

depositing and patterning a polycrystalline silicon layer over the silicon dioxide layer to form over the cavity channel a heater resistor and two other resistors, one disposed on each side of the heater resistor;

depositing and patterning aluminum to form a pair of metal pads corresponding to each resistor and interconnects from each of the metal pads to a respective end of the corresponding resistor; and

opening an inlet and outlet to the cavity channel by selectively etching locally the top silicon dioxide layer and the porous silicon layer from the substrate underneath the applied silicon dioxide layer,

to form a thermal microfluidic sensor.

23. (new) The method of claim 22, further comprising:

forming a passivation layer on top of the sensor.

24. (new) The method of claim 23, wherein the passivation layer comprises a material selected from the group consisting of silicon oxide, silicon nitride, and polyimide.

25. (new) A thermal microfluidic sensor fabricated by the method of claim 22.

26. (new) A processed silicon article, comprising:

a bulk crystalline layer comprising a cavity disposed therein in the vicinity of a first outer surface of the crystalline layer and a localized porous silicon membrane disposed over the cavity, the outer surface of the porous silicon membrane aligned with the first outer surface of the crystalline layer.

27. (new) The article of claim 26, further comprising:

a thin dielectric layer disposed on the first outer surface of the crystalline silicon layer, having the porous silicon membrane;

a patterned polycrystalline silicon layer disposed on the dielectric layer, at least one portion of the patterned polycrystalline silicon disposed over the cavity;

a first portion of the patterned polycrystalline silicon layer comprising p-doped polycrystalline silicon, to form a resistor heater;

a second portion of the patterned polycrystalline silicon layer comprising p-doped polycrystalline silicon, to form a thermocouple;

a second thermocouple disposed on the dielectric layer, said thermocouple comprising patterned aluminum or patterned n-doped polycrystalline silicon; and

pairs of aluminum metal pads and respective interconnects from the thermocouples and resistor heater to the pairs of respective aluminum metal pads, respectively, disposed on the dielectric layer.

28. (new) The article of claim 27, wherein the thermocouples comprise hot contacts and cold contacts, and wherein the polycrystalline silicon resistor and hot contacts of the thermocouples are disposed over the porous silicon membrane and the cold contacts of the thermocouples are disposed over bulk crystalline silicon.

29. (new) The article of claim 28, wherein the interconnects and metal pads are disposed over bulk crystalline silicon.

30. (new) The article of claim 26, wherein the cavity has the shape of a channel and further comprising:

a thin silicon dioxide layer disposed on the first outer surface of the crystalline silicon layer, having the porous silicon membrane;

a patterned polycrystalline silicon layer disposed on the silicon dioxide layer forming over the cavity channel a heater resistor and two other resistors, one disposed on each side of the heater resistor;

a pair of metal aluminum pads disposed on the silicon dioxide layer and corresponding to each resistor;

aluminum interconnects disposed on the silicon dioxide layer and connecting each of the metal pads to a respective end of a corresponding resistor; and

an inlet opening through the top silicon dioxide layer and the porous silicon layer to the cavity channel on one side of the resistors; and

an outlet opening through the top silicon dioxide layer and the porous silicon layer to the cavity channel on another side of the resistors.